Lab report For Lab 3 of EECS 31L 2019 Fall

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Lab Session Hours: LAB A2 16442 M 6:00 – 8:50 P.M.

T.A.: CHOOKHACHIZADE.M.

All of the files are working properly.

Objective :

This lab\_3 is asking us to design a mod 32 up& down counter. What I did is using behavioral structure to design the counter. By using if to determine if DIR is 0 or 1, if EBL is acting high and whether the CLR is active. To add std\_logic\_vector, I use IEEE.numeric\_std.all to convert makes to vector into unsigned 5 bits binary and then convert vector into int to achieve increment and decrement function and then to unsigned and finally convert back to vector to display it in the simulation flow.

Code for mod32 up/down counter:

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity Count32 is

-- Port ( );

port(

CLK : IN STD\_LOGIC;

CLR : IN STD\_LOGIC;

EBL : IN STD\_LOGIC;

DIR : IN STD\_LOGIC;

QOUT : BUFFER std\_logic\_vector(4 downto 0)

);

end Count32;

architecture Behavioral of Count32 is

begin

process(CLK,DIR,CLR,EBL)

begin

IF(EBL = '1')THEN

IF(CLK'EVENT AND CLK ='1')THEN

if(CLR = '1') THEN

QOUT <= "00000";

elsif (DIR ='0' and ebl = '1' and clr ='0') then

QOUT <= std\_logic\_vector(to\_unsigned(to\_integer(unsigned( QOUT )) + 1, 5));

elsIF(DIR = '1' and ebl = '1' and clr = '0') then

QOUT <= std\_logic\_vector(to\_unsigned(to\_integer(unsigned( QOUT )) - 1, 5));

end if;

end if;

end if;

end process;

end Behavioral;

code for mod32\_tb: (DIR is set to 1 as decrementing for this tb, the screenshots will be both up and down count)

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity tb\_count32 is

-- Port ( );

end tb\_count32;

architecture Behavioral of tb\_count32 is

component Count32 is

port (

CLK : IN STD\_LOGIC;

CLR : IN STD\_LOGIC;

EBL : IN STD\_LOGIC;

DIR : IN STD\_LOGIC;

QOUT : BUFFER std\_logic\_vector(4 downto 0)

);

end component;

signal CLK,CLR,EBL,DIR: STD\_LOGIC;

signal QOUT: std\_logic\_vector(4 downto 0);

begin

uut : Count32

port map(

CLK => CLK,

CLR => CLR,

EBL => EBL,

DIR => DIR,

QOUT => QOUT

);

clock\_proces : process

begin

wait for 40ns;

if CLK = '0' then

CLK <= '1';

else

CLK <='0';

end if;

end process;

stim\_proc:process

begin

CLR <= '0';DIR <= '1';

wait for 40 ns ;

EBL <= '1';

wait for 559ns;

ebl <= '0';

wait for 300 ns;

ebl <= '1';

wait for 50 ns;

clr <= '1';

wait;

END PROCESS;

end Behavioral; Output windows for mod32 both up and down count:

Up count:A screenshot of a computer

Description automatically generated

Down count:A close up of a computer

Description automatically generated

Code for mod21 UP/DOWN counter:

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity Count21 is

-- Port ( );

port(

CLK : IN STD\_LOGIC;

CLR : IN STD\_LOGIC;

EBL : IN STD\_LOGIC;

DIR : IN STD\_LOGIC;

QOUT : BUFFER INTEGER RANGE 0 TO 21

);

end COUNT21;

architecture Behavioral of Count21 is

begin

process(CLK,DIR,CLR,EBL)

begin

IF(EBL = '1')THEN

if(CLR = '1') THEN

QOUT <= 0;

elsif (CLK'EVENT AND CLK ='1'AND CLR ='0')THEN

if (DIR ='0') then

QOUT <= QOUT + 1;

elsIF (QOUT > 21 and DIR ='0')THEN

QOUT <= 0;

elsIF(DIR = '1' and qout>0) then

QOUT <= QOUT - 1;

else

qout<=21;

end if;

end if;

END IF;

end process;

end Behavioral;

Tb\_mod21 code(the DIR has been set to ‘1’ for down count in the tb, the screenshots contains both up and down count simulation):

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity tb\_count21 is

-- Port ( );

end tb\_count21;

architecture Behavioral of tb\_count21 is

component Count21 is

port (

CLK : IN STD\_LOGIC;

CLR : IN STD\_LOGIC;

EBL : IN STD\_LOGIC;

DIR : IN STD\_LOGIC;

QOUT : BUFFER INTEGER RANGE 0 TO 21

);

end component;

signal CLK,CLR,EBL,DIR: STD\_LOGIC;

signal QOUT: INTEGER RANGE 0 TO 21;

begin

uut : Count21

port map(

CLK => CLK,

CLR => CLR,

EBL => EBL,

DIR => DIR,

QOUT => QOUT

);

clock\_proces : process

begin

wait for 40ns;

if CLK = '0' then

CLK <= '1';

else

CLK <='0';

end if;

end process;

stim\_proc:process

begin

CLR <= '0';

DIR <= '1';

wait for 40 ns ;

EBL <= '1';

wait for 599ns;

EBL <= '0';

WAIT FOR 300NS;

EBL <= '1';

WAIT FOR 200NS;

CLR <= '1';

WAIT;

END PROCESS;

end Behavioral;

MOD21 UP/DOWN COUNTER SCREENSHOTS:

Up count:

A close up of a computer

Description automatically generated

Down:

A close up of a computer

Description automatically generated